TRIBHUVAN UNIVERSITY
FACULTY OF MANAGEMENT
Office of the Dean

April 2019

Full Marks: 40
Pass Marks: 20
Time: 2 Hrs.

BIM / First Semester / ITC 212: Digital Logic / IT 212: Digital Logic Design

Candidates are required to answer all the questions in their own words as far as practicable.

Group "A"

Brief Answer Questions: *[10 × 1 = 10]*

1. Why alphabets are used for representing number above 9 in hexadecimal number system?
2. Why NAND gate is said to be universal gate?
3. How many don't cares are there in 10×4 encoder?
4. Define noise immunity of IC.
5. What is the use of cascaded Counter?
6. What will be the state of twisted ring counter after 4th clock pulse if its initial state is 1001001?
7. How combinational circuit is recognized?
8. If the word size of a memory is 32-bit and size of memory is 2GB then what will be the size of address decoder?
9. Draw PLA circuit for expression AB + CD.
10. Define coarse grained FPGA.

A'B'C'D

Group "B"

Short Answer Questions: *[5 × 4 = 20]*

11. Explain Setup time, Hold time, Propagation delay, Power dissipation and Maximum clock frequency of flip flop.
12. You are provided with data bits 101101 to operate in a register which supports I/O (single bit per clock pulse) from either side of it. Also draw timing diagram to illustrate store / retrieve operation.
13. Draw state diagram and construct state table for sequence recognizer machine which recognizes bit pattern 11001.
14. Design 10×1 Multiplexer using only NOR gates.
15. (a) Convert 2040.0001953125_{10} to binary, octal and hexadecimal number system.

    (b) Add: $(-111_{10}) + (-27_{10})$ using signed 2's complement data.

Group "C"

Long Answer Questions: *[2 × 5 = 10]*

16. Convert given SOP expression: $\bar{A}BC + AB\bar{C}D + AB\bar{D} + \bar{A}\bar{B}\bar{D} + C\bar{D} + A\bar{B}D + B\bar{D}$ to POS expression and draw circuit of minimized expression using minimum number of NAND gates.
17. Design synchronous counter which generates odd numbers from 0 to 15.

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