TRIBHUVAN UNIVERSITY
FACULTY OF MANAGEMENT
Office of the Dean
April 2018

Full Marks: 40
Time: 2 Hrs.

BIM / First Semester / ITC 212: Digital Logic / IT 212: Digital Logic Design

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Candidates are required to answer all the questions in their own words as far as practicable.

Group "A"

Brief Answer Questions: [10 × 1 = 10]

1. What do you mean by truncated counter?

2. Differentiate between latch and flip-flop

3. What are the purposes of adder and subtractors?

4. Differentiate between PLA and ROM.

5. Which flip-flop can complement the state if input gives high and clock is enabling?

6. Why do we need don't cares in K-map?

7. If T-flip flop have input 0&1 when the present state are respectively 0&1 what will be the output in both cases?

8. If the state of Johnson counter is 1101 what will be the state after 7th clock pulse?

9. "Flip-flop is 1 bit memory". Justify

10. List the advantage of PLDS over Fixed function devices.

Group "B"

Short Answer Questions: [5 × 4 = 20]

11. (a) Convert the decimal number 2.5 to equivalence binary number.

    (b) Differentiate between min-term and max-term.

12. You need to store binary information 0101 by shifting right and extract those bits by shifting left, which shift register will you suggest? Design your suggested shift register with operational table and timing diagram.

13. Design a combinational circuit that take 3 bit input and output is generate 1's complement of its input using NOR gate only.

14. Design decade asynchronous counter with operational table and timing diagram.

15. Design and explain the operational characteristics of flip-flop which solved the problem of clocked JK flip-flop.

Group "C"

Long Answer Questions: [2 × 5 = 10]

16. Simplify the Boolean expression $F(A,B,C,D) = \sum (1,2,4,6,7,11,12,13)$ and don't care conditions $D(A,B,C,D) = \pi (0,15)$ in POS and realized it with minimum no of NAND gate.

17. Design a sequence detector whose output is 1 when a pattern found 0101 using D flip-flop.