# TRIBHUVAN VUNIVERSITY

FACULTY OF MANAGEMENT Office of the Dean

### March – April 2017

# BIM / First Semester / ITC 212 : Digital Logic / IT 212: Digital Logic Design

Candidates are required to answer all the questions in their own words as far as practicable.

# Group "A"

# **Brief Answer questions :**

- Express FOM in ASCII code. 1.
- Why gray codes are used in K-map instead of binary code? 2
- What is the maximum number of half adder that we can use in n bit parallel adder and why? 3.
- 4. Identify and state the similarity between latch and flip- flop.
- What is the use of cascaded counters? 5.
- Which shift register counter constructed using "n" flip flop can "2n" states and why ? 6.
- 7. If the size of address register is 4 –bit then what will be the maximum number of words that can be stored in memory?
- 8. Differentiate between fine grained and coarse grained FPGA.
- 9. Define noise immunity.
- 10. Differentiate between Truth table and Characteristics table.

#### Group "B"

# Short Answer Questions:

- 11. State and prove distributive law using truth table method. (a)
  - If  $A = (1011)_2$ , then perform A-B using signed 2's Complement method. (b)
- 12. Design and explain the operational characteristics of flip flop that is single input version of JK flip flop.
- 13. Design circuit that can display 2,5,7 and E in seven segments.
- 14. Design 3-bit asynchronous UP/DOWN counter.
- 15. Design and explain a shift register where 4 bit data be simultaneously loaded in a single clock pulse and data can be shifted one bit at time from it.

#### Group "C"

#### Long Answer questions:

- If F=(A'+B)(A+D)(A+B'+C)(A'+B'+C'+D') then minimize it using 16. K-map and design a circuit using minimum numbers of NAND gates.
- 17. Design circuit of sequence recognizer that detects the bit sequence 11111.

#### https://genuinenotes.com

# [10\*1=10]

# [5\*4=20]

[2\*5=10]

Time: 2hrs

Full Marks: 40