TRIBHUVAN UNIVERSITY
FACULTY OF MANAGEMENT
Office of the Dean
2016

Full Marks: 40
Time: 2 hrs.

BBA/BIM/ First Semester/IT 212: Digital Logic Design

Candidates are required to answer the questions in their own words as far as practicable

Group 'A'

Brief Answer Questions: ***[10×1=10]***

1. Mention the disadvantages of parity method of error detection.
2. Minimize ZX+ZX'Y to minimum number of literals using Booelean rule.
3. It is possible to design a combinational circuit that adds two 3-bit numbers using only half adder? Support your answer.
4. What is the advantage of flip flop over latch?
5. Why BCD counters is define as truncated counter?
6. What is the strength of Johnson counter over Ring counter?
7. What are the symbols used in state diagram?
8. What is the importance of refreshing circuit in DRAM?
9. Differentiate between CPLD and SPLD.
10. Which logic family of IC will be suitable for circuit requiring wide range of dc supply voltage and why?

Group 'B'

Short Answer Questions: **[5×4=20]**

11. (a) If F = AB + A'B and F2 = A'B + A'B'; then design PLA that produce F1 and F2.
    (b) If A = -14 and B = 9, then calculate A-B using signed 2' s Complement data.
12. Design and explain the flip flop which complements its present state when the clock is triggered with both input HIGH.
13. Design 12x1 multiplexer using minimum number of NAND gates.
14. Design a 3 bit synchronous counter using T flip flop that counts only even sequences.
15. You have five bit data: 11001 which is to be loaded in a register simultaneously, ad you are asked to shift those bits one bit at a time. Which shift register will you use? Explain with necessary diagrams.

Group 'C'

Long answer questions: **[2×5=10]**

16. If f (P,Q,R,S) = II(0,1,4,5,11,14,15) and d (P,Q,R,S) =II(2,3,7,8,9,13), then design circuit using minimum number of NOR gates and basic gates.
17. Design a sequence recognizer circuit using D flip flop that recognize the sequence 11101.