TRIBHUVAN UNIVERSITY
FACULTY OF MANAGEMENT
Office of the Dean
2014

Full Marks: 40
Time: 2 hrs.

BIM/ First Semester/IT 212: Digital Logic

Candidates are required to answer the questions in their own words as far as practicable

Group "A"

Brief Answer Questions: **[10×1=10]**

1. Differentiate periodic and non periodic wave.
2. Decimal numbers are weighted numbers. Justify.
3. What is the number selection line if multiplexer have 1234 input lines?
4. How many Flip-flops are required to divide a frequency by 16?
5. It is possible to implement counting function using data flip-flop? Support your answer.
6. If the state of 4-bit Johnson counter is 1100, what is its state after 4^{th} clock pulse?
7. How size of data register and address register are calculated in computer system?
8. Write advantages of PLA over ROM.
9. Explain any operational characteristics of an IC.
10. Define Excitation table.

Group "B"

Short Answer Questions: **[5×4=20]**

11. a. If $A = 15_{10}$ and $B = -12_{10}$ Compute B-A and A+B by converting them to binary system.
    b. Verify any one De Morgan's law for three variables using Truth Table.
12. Design circuit diagram for code converter.
13. Construct MOD – 8 asynchronous up down counter with timing diagram.
14. Discuss flip flop operating characteristics.
15. If you have five bit of data to insert into a shift register all at once and you need to extract these data one bit a time, which shift register will you suggest? Design a circuit diagram for your selection and explain its operation.

Group "C"

Long Answer Questions: **[2×5=10]**

16. If (A, B, C, D) = $\sum$ (3 , 4, 7, 8, 14) and d(A, B, C, D) = $\sum$ (1, 6, 9, 13) design a truth table for this expression and design a circuit using
    a) Using Basic gates
    b) Using minimum number of NAND gates.

17. Analyze the following sequential circuit.