TRIBHUVAN UNIVERSITY
FACULTY OF MANAGEMENT
Office of the Dean
2011

Full Marks: 40
Time: 2 hrs.

BIM/ First Semester/ITC 212: Digital Logic

Candidates are required to answer the questions in their own words as far as practicable

Group 'A'

Attempt All questions:

Brief Answer Questions: **[10×1=10]**

1. Write one application area of I^2L and ECL.
2. Simplify: P'Q' + PQ + QP' + PQR'S'.
3. Convert $(AB.0F)_{16}$ to Binary.
4. Write the advantage of BCD code.
5. What is the output frequency if the input frequency to the Mod-8 counter is 800 Hz?
6. What is the weight of 1 in binary number 0.0000100?
7. Draw the logic symbol of AND and OR gate used in PAL and PLA.
8. List the levels of integration.
9. What is the advantages of Johnson Counter over Ring Counter?
10. What is the minimum number of inverters required to find the 1's complement of $(101011100)_2$

Group 'B'

Short Answer Questions: **[5×4=20]**

11. **a.** If A=127 and B=15, then calculate (-A) + (-B) using 2's complement concept.
    b. Compare Analog and Digital signal.
12. Make distinction between RS and D flip flop along with its circuit diagram, characteristic equation and characteristic table.
13. You are provided with a bit sequence 00010 to operate with Serial In Out register. Describe the store and retrieve mechanism with supportive diagram and also draw the timing diagram.
14. Draw the circuit diagram of half adder and 1×4 Demultiplexer.
15. Design an asynchronous MOD-03 counter.

Group 'C'

Long Answer Questions: **[2×5=10]**

16. Draw the circuit diagram to represent the given K-map using:
    a) AND-OR-NOT gate
    b) Minimum number of NOR gates.

R \ PQ	00	01	11	10
0		×	1	1
1	1		×	1

17. Design a synchronous sequential circuit using D flip flop with one input P and an output Q. The input P is a serial message and the system reads P one bit at a time. The output Q=1 whenever the pattern 000 is encountered in the serial message.

https://genuinenotes.com