TRIBHUVAN UNIVERSITY
FACULTY OF MANAGEMENT
Office of the Dean
2009

Full Marks: 40
Time: 2 hrs.

BIM/ First Semester/ITC 212: Digital Logic

Candidates are required to answer the questions in their own words as far as practicable

Group 'A'

Attempt All questions:

Brief Answer Questions: **[10×1=10]**

1. Define a Clock Pulse ?
2. What are error detection codes? Give an example.
3. Differentiate between LCD and LED.
4. What is the weight of 0 in binary number 10111?
5. How many Full Adders and Half Adders are required if you want to add 2 four bit words?
6. Describe PLA with a simple example of your choice.
7. Differentiate Combinational circuit from Sequential Circuit.
8. Suggest a circuit to obtain 1 Hz pulse if you are provided with 16 Hz pulse. Draw the necessary timing diagrams.
9. A Memory device has 500 distinct memory locations. How many address line are required?
10. List the properties of TTL.

Group 'B'

Short Answer Questions: **[5×4=20]**

11. **a.** If A=61 and B=32, Represent them in Binary and perform B-A. (Use 2's complement)
    b. Explain briefly about the process involved in Analog to digital conversion.
12. A multiplexer has 99 inputs. How many select lines are required? Construct 8 to 1 Multiplexer using 4 to 1 Multiplexers.
13. Draw the circuit diagram of a J-K Flip Flop along with its Truth Table and Characteristic equation.
14. You are provide with a bit sequence 101, and you are asked to extract those bits after right shifting. Which shift register would you use? How many Clock Pulses would it consume? Discuss with necessary block diagrams and timing diagrams.
15. Design an Asynchronous MOD-12 Counter.

Group 'C'

Long Answer Questions: **[2×5=10]**

16. Simplify the following using k-map
    Y=(ABCD') + (A'B'CD) + (ABC) + (A'B'C'D') + (ACD) + (AB'C'D) and draw' circuits using:
    a. AND – OR gates
    b. NAND gates only.
    You can use Not Gates wherever necessary.
17. **a**. Draw the circuit diagram of a Digital Clock.
    b. You are provided with a sequence 011, at the end of this sequence, the output of the Sequential Machine should be at logic 1. Draw the State Diagram and State Table for your machine.