TRIBHUVAN UNIVERSITY
FACULTY OF MANAGEMENT
Office of the Dean
April - May 2017

Full Marks: 40
Time: 2 hrs.

BIM / Third Semester / IT 217: Computer Organization

Candidates are required to answer all the questions in their own words as far as practicable.

Group "A"

Brief Answer Questions: *[10 × 1 = 10]*

1. What is the advantage of normalized floating point number?
2. Why control data register in micro-programmed control organization is called pipeline register?
3. What are the different techniques used to achieve parallel processing?
4. Differentiate between address space and memory space.
5. Why interrupt initiated I/O is better than programmed I/O techniques?
6. Why peripherals are connected with computer through interface?
7. Write microinstruction format of basic computer.
8. Why hierarchy of memory is maintained?
9. Differentiate between vector and array processor.
10. Define cache coherence.

Group "B"

Exercise Problems: *[5 × 4 = 20]*

11. Perform the arithmetic operations (+33) + (+48) and (-33) + (-48) with binary numbers in signed 2's complement representation. Use seven bits to accommodate each number together with its sign. Show that overflow occurs in both cases.
12. Explain how instruction is executed in basic computer with necessary flow chart.
13. The time delay of the four segments in the pipeline system are $t_1 = 30ns$, $t_2 = 35ns$, $t_3 = 20ns$ and $t_4 = 45ns$. The interface registers delay time $d = 4ns$. Find the speed up ratio of pipeline system over equivalent conventional system for 100 tasks.
14. Write a symbolic program to subtract two double precision numbers and explain each statement.
15. Multiply (-37) × (+13) using "**multiplication of signed 2's complement data**" algorithm.

Group "C"

Comprehensive Answer Questions: *[2 × 5 = 10]*

16. What are the different CPU organizations? List and explain each type of addressing modes available.
17. Explain hypercube interconnection structure in brief with its merits and demerits. Explain different cache mapping techniques.

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