TRIBHUVAN UNIVERSITY
FACULTY OF MANAGEMENT
Office of the Dean
2015

Full Marks: 40
Time: 2 hrs.

BIM / Third Semester / IT 217: Computer Organization

Candidates are required to answer all the questions in their own words as far as practicable.

Group "A"

Brief Answer Questions: *[10 × 1 = 10]*

1. Define the term normalization with respect to a floating point numbers.
2. Write down the symbolic designation of a shift microoperation where the shifting is carried out without loss of information.
3. How I/O instruction is identified in a basic computer?
4. Make distinction between RISC and CISC architecture.
5. Write down the uses of sequencer in a miroprogrammed control organization.
6. How is effective address calculated in indexed register addressing mode?
7. List solutions to control hazards.
8. What is the disadvantage of programmed I/O?
9. Differentiate between logical address and virtual address.
10. Define associative memory.

Group "B"

Exercise Problems: *[5 × 4 = 20]*

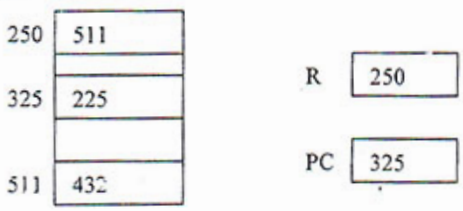
11. The 4-bit registers A, B, C and D initially have the following values:

    A = 0010, B = 0111, C = 1000, D = 1111

    Determine the 4-bit values in each register after the execution of the following sequence of micro-operations.

    A←A + C
    C←C ∧ D, D←D + 1
    A←A - B

12. Write a program to take two integers and display them.
13. Time taken to complete a task in conventional machine is 45ns. In pipelined machine, one task is divided into 5 segments and each sub-operation takes 10ns. Calculate pipeline speed up for 50 tasks and infinite tasks.
14. Consider the following memory and the instruction LDA 250:



    Write the value loaded into AC when the addressing mode is

    a) Indirect b) Register Indirect c) Immediate d) Direct

15. Multiply +15 by -5 using booth algorithm.

Group "C"

Comprehensive Answer Questions: *[2 × 5 = 10]*

16. Explain how data is transferred using handshaking methods? Explain interrupt cycle of Basic Computer.

17. Explain any two interconnection structures for a multi-processor. Explain cache mapping techniques.

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